

Results 2010

Table of Contents

1 Executive summary	1
2 Approach	2
2.1 Materials	2
2.2 Processes	2
2.3 Products	2
3 Results 2010	2
3.1 Materials	2
3.1.1 Crystallization and Wafering	2
3.1.2 Cell processing	3
3.1.3 Module	4
3.2 Processes	4
3.3 Products	7
4 Outlook	8
5 Acknowledgement	8

1 Executive summary

The International Technology Roadmap for Photovoltaic (ITRPV) organized by the Crystalline Silicon Technology and Manufacturing (CTM) Group* aims to inform suppliers and customers about expected technology trends in the field of crystalline silicon (c-Si) photovoltaics and sets a basis to intensify the dialog on required improvements and standards. The present second edition of the ITRPV was jointly prepared by leading European c-Si solar cell manufacturers, module manufacturers, and wafer suppliers.

More information is available on www.itrpv.net.

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*Crystalline Silicon Technology and Manufacturing (CTM) Group

































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2 Approach

It has been essential to gather data for the roadmap. The participating companies active along the value chain from crystallization to the building of modules jointly agree on the parameters to be reported in the roadmap publication. Data preparation is done by anonymously summarizing the input of each company. The expected trends up to the year 2020 are shown in graphs and for some parameters color marking is used to indicate the maturity of the technology today (see Table 1). All parameters are median values and answers are given based on data from the latest generation production line.

The topics are split into three areas: materials, processes and products. Within these groups we will discuss details for wafer, cell and module respectively.

Table 1: Color marking

Green	Industrial solution exists and is being optimized in production.
Yellow	Industrial solution is known but not yet in production.
Orange	Interim solution is known, too expensive or not suitable for production.
Red	Industrial solution is not known.

2.1 Materials

Requirements and trends concerning raw materials and consumables used within the value chain are described in this section. A replacement of some materials will be necessary to secure availability, avoid environmental risks, reduce costs and increase efficiency. Price development plays a major role in reaching the goal of grid parity and is discussed for selected topics.

2.2 Processes

To reduce production costs, new technologies, materials and highly productive equipment including Statistical Process Control (SPC) are needed. By giving information on important key figures of the production, as well as details of the process to increase the cell efficiency and finally the power output of the modules, the roadmap will be the guideline to support these developments. In the process chapter we identify manufacturing and technology topics for each section of the value chain. Manufacturing focuses on increased productivity while technology developments have to ensure higher cell and module efficiencies.

The analysis demonstrates clearly that the reduction of manufacturing costs per Wp are dominated by the reduction of the manufacturing costs per piece of wafer, cell, and module (assuming a constant cell areal while the contribution of increased cell efficiency is less pronounced. Only a combination of increased module conversion efficiency and significantly reduced manufacturing costs will enable the PV industry to reach the overall cost targets.¹

2.3 Products

Each part of the value chain has its respective final product. The chapter "Products" discusses the development of the key features for wafers, c-Si solar cells, and modules over the next years.

3 Results 2010

3.1 Materials

3.1.1 Materials- Crystallization and Wafering

The costs for the material have a significant influence on the total costs. To be able to reach the overall goal of cost reduction the price of silicon needs to be reduced by 50% until the year 2020 as shown in Fig 1.

¹ See als full version of the ITRPV

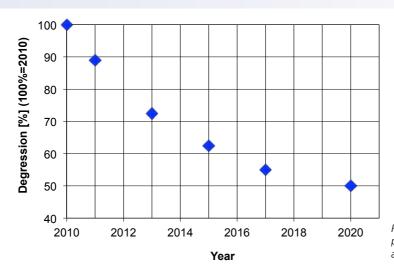


Fig 1: Required price degression of pure poly-silicon. The chart does not include availability-related fluctuations.

3.1.2 Materials - Cell processing

The most expensive material in cell processing is the silicon wafer. Thus reducing the wafer thickness reduces the material cost. Wafers will become thinner, though not as fast as predicted in the first roadmap edition. Fig 2 shows the expected trend of thinnest wafers processed in mass production. Thickness reduction is postponed by 2 years compared to the first edition, mainly because the higher availability of silicon feedstock led to a significant reduction of wafer prices and reduced the pressure to minimize silicon consumption. Wafers with the current standard format (156x156 mm²) remained the norm until 2020; larger wafers (210x210 mm²) are expected to appear in production earliest 2017.

Slicing of 100 μ m wafers is possible from the point of wafer slicing technology but with an unacceptable yield loss so far. The red color-coding in Fig 2 addresses this issue.

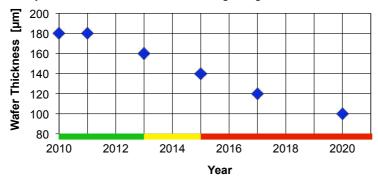


Fig 2: Trend of minimum wafer thickness processed in mass production of solar cells.

Silver and aluminum are identified as a major cost driver in the metallization process. Therefore paste consumption needs to be reduced in a first step. Fig 3 shows our estimations for the reduction of silver for 156x156 mm² cells. In a second step silver shall be replaced on a large-scale basis starting in 2015. Cu is intended to be the substitute.

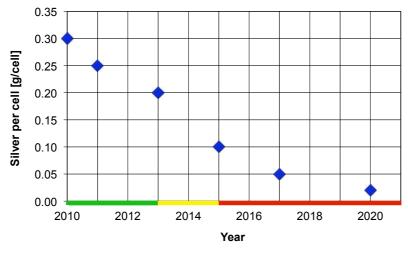


Fig 3: Remaining portion of silver per cell. A technological development in 2015 is expected to replace silver with Cu.



3.1.3 Materials - Module

Looking at the module cost structure there are also materials that need to be improved in performance and reduced in price. The reflectivity at the front side of the glass-air interface will be reduced from typically 4% to 2% by introducing anti-reflection glass from 2013 onwards into the mainstream as shown in Fig 4. The absorbance in glass and encapsulant need to be reduced to minimize the cell-to-module power loss.

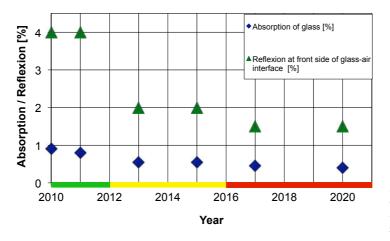


Fig 4: Requirements for the absorption of glass, as well as reflection at the front side of the glass-air interface.

The consumables frame, glass, encapsulant, back sheet foil and junction box have about equal cost contributions in the distribution of costs. All materials should therefore contribute equally to the ongoing reduction in module manufacturing costs.

3.2 Processes

Increasing the throughput of the crystallization process is possible by changing common formats of the ingots. The roadmap predicts an increase in ingot mass for monocrystalline silicon (mono-Si) and for multicrystalline silicon (mc-Si). In addition, the ingot height as well as the ingot footprint for mc-Si will rise respectively as shown in Fig. 5.

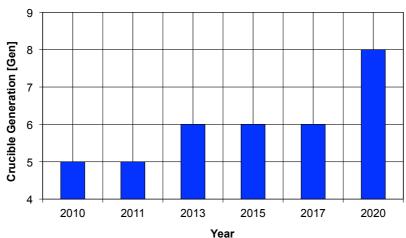


Fig. 5: Trend of mc-Si ingot footprint showing the type of crucible generation used in the newest production lines (mc-Si only).

According to the economy of scale the productivity of tools needs to improve by increasing yield and throughput of a production line resulting in the reduction of labor cost and tool cost per product.

Fig. 6 shows that by 2020, mechanical yield loss in the cell production is expected to decrease to below 1%. Note that, at the same time, this includes introduction of thinner wafers..

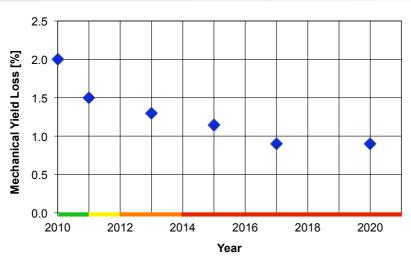


Fig. 6: Mechanical yield loss during cell processing needs to be reduced significantly over the next years.

The tool uptime based on the SEMI Standard E10 is another important factor for optimizing the production lines. To enable uptimes of above 96% as shown in Fig. 7, there is a particular need for improvements in the process groups metallization and classification. Those values have to be seen as minimum requirements — even tools with higher uptime values are preferred.

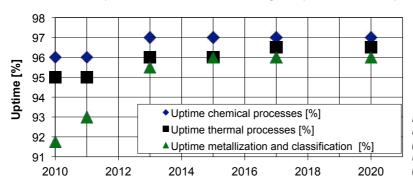


Fig. 7: Tool uptime needs to be improved. There is a high potential for improvements in the metallization and classification process group.

Fig. 8 shows the expected reduction of invest for new cell fabs per MWp as result of the improvements in manufacturing technologies and equipment. This data is based on the input from the participating cell manufacturing companies.

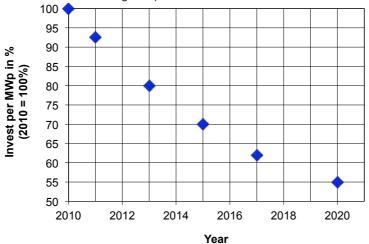


Fig. 8: Chart showing the relative invest per MWp for a c-Si cell production line.

To achieve the required cost reductions, module-manufacturing equipment should occupy less floor space (see Fig 9) and have a higher throughput. A higher throughput can be achieved by a combination of continuous improvement and new developments, particularly for the interconnection and encapsulation processes.

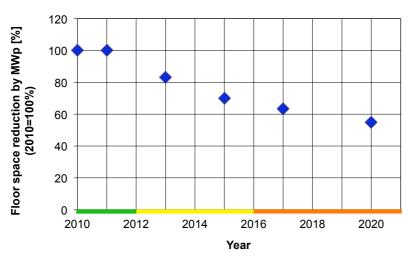


Fig 9: Expected floor space reduction per MWp output in module manufacturing equipment

Another challenging parameter as shown in Fig. 10 is the kerf loss. Following the wafer thickness reduction the kerf loss must also be decreased accordingly to achieve a significant reduction in silicon consumption.

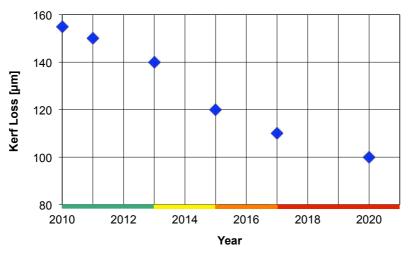


Fig. 10: Kerf loss reduction trend expected by the roadmap.

Solar cell recombination losses in at front and rear side oft he crystalline Si bulk material, must be reduced. A reasonable way to describe the recombination losses are the recombination currents Jobulk, Jofront, Jorear that describe the recombination losses in the volume, at the cell front side, and at the cell rear side respectively. Fig.11 shows that all recombination currents need to be reduced.

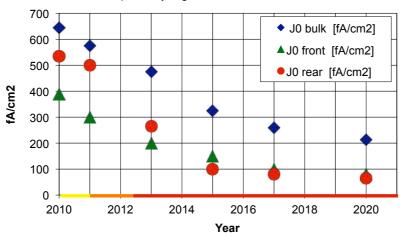


Fig.11: Trend of recombination currents JObulk, JOfront, JOrear.

The recombination current can be measured as described in literature (Kane, 1985) 1 or extracted from the IV curve, if other JO components are known. By 2012 new processes with lower Cost of Ownership (CoO) and

¹ Kane, IEEE PV Sec, 18 (1985)

better passivation properties, compared to current technologies, will be needed. Values below 200 fA/cm² cannot be reached with an Al Back Surface Field (BSF). In addition rear side reflection also needs to improve.

It is crucial to get as much power out of the assembled solar cells as possible I. A good parameter expressing this is the module-to-cell power ratio, defined as module power divided by cell power times number of cells (module power/cell power x number of cells). As shown in Fig 12, this ratio is currently around 97.5% for multi crystalline silicon cell technology and 96% for mono crystalline silicon cell technology. In 2013, the power ratio will show an improvement of +1.5% abs. due to the introduction of AR glass (see Fig 4). The introduction of new interconnection and encapsulation technologies (for back contacted cells and thin wafers) will result in a second improvement step of about +1.0% abs from 2015 onwards.

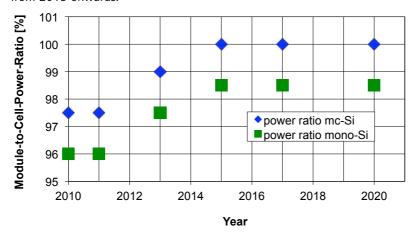


Fig 12 Expected trend of module-to-cell power ratio.

3.3 Products

Due to the current interconnection and lamination technology, bow is an important parameter for the module manufacturer. To ensure high yields, it must be lower than 2 mm. This restriction will remain at least until 2015 when new interconnection and lamination technologies that are especially designed for handling of wafers with a thickness below 150 μ m will be introduced. The cell bow restrictions for these new interconnection and lamination technologies still need to be defined. It is expected that the cell bow will decrease to 1.5 mm in 2020 due to novel cell technologies being implemented.

The share of n-type mono wafers is expected to increase over the next few years starting at about 8% today to a share of up to 50% in 2020, as shown in Fig. 13. We expect less market share for n-type multi wafers.

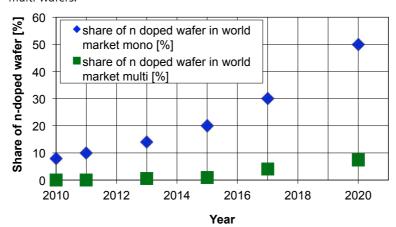


Fig. 13: Expected share of n-type material on world production of c-Si solar cells.

Over the next years, the efficiency of p-type mc-Si solar cells will increase. Fig. 14 shows the expectation of average stabilized efficiencies for mc-Si and mono-Si solar cells in a state of the art mass production line. Fig. 15 shows the corresponding development of the module power [W] considering that there will be a transition in mono-Si wafers format from semi square to full square starting in 2015.

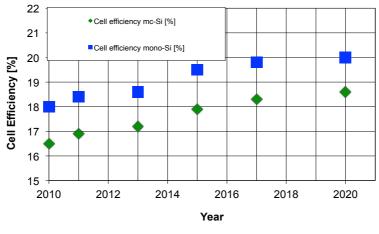


Fig. 14: Stabilized efficiency trend curve of p-type c-Si solar cells in mass production.

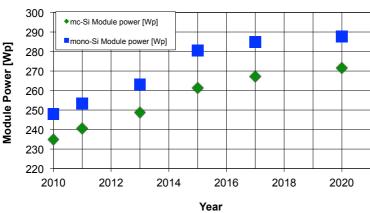


Fig. 15 Output power of 60 cell modules corresponding to the efficiency development shown in Fig. 28

4 Outlook

This data was collected from the leading European manufacturers along the c-Si value chain in 2010. A yearly update of this information is planned. Topics such as wafer size require cooperation between suppliers, cell manufacturers and other players along the value chain. The download of the current issue of this document as well as information about how to get involved in the roadmap activity are available on the website www.itrpv.net

5 Acknowledgement

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